Appl. No. 09/902,277

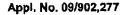
REMARKS

Claims 51-58 are pending in the application. Claims 51-58 correspond directly to claims pending as of the response to the April 10, 2002 Office Action dated. No amendments have been made relative to the previous response, however the claims have been renumbered to overcome confusion as to the claim numbering as indicated by the Examiner in the present Action. All previous versions or previous numbering of any pending claim is cancelled.

The arguments set forth in the remarks section of the Response to the April 10, 2002 Office Action are re-iterated below as set forth in the previous response with the exception that the arguments reference the claims as renumbered herein. Applicant respectfully requests examination of the claims as newly renumbered.

Claims 51-55 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nishimura et al., U.S. Patent No. 5,440,168. The Examiner is reminded by direction to MPEP § 2131 that anticipation requires each and every element of a claim to be disclosed within a single prior art reference. Claims 51-55 are allowable over Nishimura for at least the reason that Nishimura fails to disclose each and every limitation in any of those claims.

Independent claim 51 recites forming a fluorine-containing layer proximate a polycrystalline thin film transistor layer, the fluorine-containing layer comprising tungsten. The subject matter recited in claim 51 is supported by the specification at, for example, page 9, lines 10-23. Nishimura discloses implanting fluorine into a polysilicon gate electrode (col 8, lns 24-27), implanting fluorine into



a channel polysilicon layer (col 9, Ins 48-51), implanting fluorine into the drain region of a polysilicon thin film (col 11, Ins 18-21) or implanting fluorine into an active region of a polysilicon thin film (col 11, Ins 51-61). The Examiner states at paragraph 1 of page 3 of the present action that Nishimura teaches forming a fluorine-containing layer by CVD using WF₆ and directs attention to Nishimura at column 7, lines 1-10. Applicant notes that at column 7, lines 1-10, Nishimura discloses CVD formation of a silicon oxide film utilizing N₂ and SiH₄. Nishimura does not disclose or suggest the claim 51 recited forming a fluorine-containing layer which comprises tungsten proximate a polycrystalline thin film transistor layer. Accordingly, independent claim 51 is not anticipated by Nishimura and is allowable over this reference.

Dependent claims 52-54 are allowable over Nishimura for at least the reason that they depend from allowable base claim 51.

Independent claim 55 recites forming a fluorine-containing layer over a transistor gate and over a polycrystalline thin film transistorlayer. Claim 55 further recites transferring fluorine from the fluorine-containing layer into the polycrystalline thin film transistor layer over the transistor gate. The subject matter of independent claim 55 is supported by the specification at, for example, page 13, lines 1-11 and Fig. 8. The Examiner relies on the Nishimura disclosure at Fig. 19 and the accompanying text, and column 11, lines 25-35 to support the anticipation rejection of claim 55. Applicant notes that the implanted fluorine of Fig. 19 is implanted into a layer of resist over the gate layer and as a result is prevented from diffusing into the thin film channel region over the gate (col 11,

P.07/07 5098383424

Appl. N . 09/902,277

Ins 14-28). Nishimura does not disclose or suggest the claim 55 recited forming a fluorine-containing layer over a transistor gate and over a polycrystalline thin film transistor layer, and transferring fluorine from the fluorine-containing layer into the polycrystalline thin film transistor layer over the transistor gate. Accordingly, independent claim 55 is not anticipated by Nishimura and is allowable over this reference.

Claims 56-58 do not add "new matter" to the specification since each is fully supported by the specification as originally filed. Claim 56 is supported by the specification at, for example, page 9, lines 10-23; and page 13, lines 1-11. Claim 57 is supported by the specification at, for example, page 12, lines 12-17. Claim 58 is supported by the specification at, for example, page 9, lines 7-9.

For the reasons discussed above, claims 51-55 are allowable and claims 56-58 are believed allowable. Accordingly, applicant respectfully requests formal allowance of claims 51-58 in the Examiner's next action.

> FAX COPY RECEIVED OCT 2 2 2002

TECHNOLOGY CENTER 2800

Respectfully submitted,

Dated: October 22, 2002